EAST SEARCH SUMMARY

Hits	Search Text	DBs	Date
1	("10228497").PN.	JPO	4/24/02 10:35
0	(""9260498"").PN.	JPO	4/24/02 10:47
1	("10124565").PN.	JPO	4/24/02 10:53
1	("11154168").PN.	JPO	4/24/02 11:16
3533	hot adj carrier	USPAT; US-PGPUB	4/24/02 14:33
3293	(hot adj carrier) and (effect degradation reliability)	USPAT; US-PGPUB	4/24/02 14:43
511	((hot adj carrier) and (effect degradation reliability)) and delay	USPAT; US-PGPUB	4/24/02 14:44
338	(((hot adj carrier) and (effect degradation reliability)) and delay) and input and output	USPAT; US-PGPUB	4/24/02 14:44
3316	(hot adj carrier) and (effect degradation reliability deterioration)	USPAT; US-PGPUB	4/24/02 14:44
513	((hot adj carrier) and (effect degradation reliability deterioration)) and delay	USPAT; US-PGPUB	4/24/02 14:44
340	(((hot adj carrier) and (effect degradation reliability deterioration)) and delay) and input and output	USPAT; US-PGPUB	4/24/02 14:47
249	((((hot adj carrier) and (effect degradation reliability deterioration)) and delay) and input and output) and @ad<=19980707	USPAT; US-PGPUB	4/24/02 14:51
17	(((((hot adj carrier) and (effect degradation reliability deterioration)) and delay) and input and output) and @ad<=19980707) and (age aged)	USPAT; US-PGPUB	4/24/02 14:51

EAST Search: (hot adj carrier) and (effect degradation reliability deterioration) and delay and input and output and @ad<=19980707 and (age aged)

Document ID	Issue Day	Pages	Title	Current OR	Current Xref	Inventor
US 6278964 B1	20010821	33	Hot carrier effect simulation for integrated circuits	703/19	703/14; 714/25; 714/47	Fang, Jingkun et al.
US 6216099 B1	20010410	10	Test system and methodology to improve stacked NAND gate based critical path performance and reliability	703/15	257/344; 326/121; 438/327; 716/1; 716/4	Fang, Peng et al.
US 6047247 A	2000040[illegible]	22	Method of estimating degradation with consideration of hot carrier effects	702/117	324/769; 714/24; 714/37; 714/55	Iwanishi, Nobufusa et al.
US 5974247 A	19991026	31	Apparatus and method of LSI timing degradation simulation	703/19	703/20; 716/6	Yonezawa, Hirokazu
US 5964884 A	19991012	20	Self-timed pulse control circuit	713/503	711/167; 713/400; 713/401; 713/500; 713/501; 713/502	Partovi, Hamid et al.
US 5754714 A	19980519	41	Semiconductor optical waveguide device, optical control type optical switch, and wavelength conversion device	385/5	385/131; 385/16	Suzuki, Nobuo et al.
US 5376839 A	19941227	80	Large scale integrated circuit having low internal operating voltage	327/541	323/313; 323/315; 323/316; 327/108; 327/530	Horiguchi, Masashi et al.
US 5254880 A	19931019	78	Large scale integrated circuit having low internal operating voltage	327/530	327/100; 327/141; 327/535; 327/537	Horiguchi, Masashi et al.
US 5179539 A	19930112	81	Large scale integrated circuit having low internal operating voltage	365/226	327/537	Horiguchi, Masashi et al.
US 4994688 A	19910219	81	Semiconductor device having a reference voltage generating circuit	327/541	323/314; 323/315; 323/907; 327/331; 327/513; 327/581	Horiguchi, Masashi et al.
US 4488554 A	19841218	28	Externally-inhibited tachycardia control pacer	607/14		Nappholz, Tibor A. et al.
US 4488553 A	19841218	28	Externally controlled tachycardia control pacer	607/14		Nappholz, Tibor A. et al.
US 4407289 A	19831004	29	Externally-reset tachycardia control pacer	607/14		Nappholz, Tibor A. et al.
US 4406287 A	19830927	25	Variable length scanning burst tachycardia control pacer	607/15		Nappholz, Tibor A. et al.
US 4398536 A	19830816	24	Scanning burst tachycardia control pacer	607/15		Nappholz, Tibor A. et al.
US 4390021 A	19830628	32	Two pulse tachycardia control pacer	607/14		Spurrell, Roworth A. J. et al.
US 3882413 A	19750506	12	Microwave signal source stabilized by automatic frequency and phase control loops	331/9	331/12; 331/25	Healey, III, Daniel J.